Microchip

28C64B

64K (8K x 8) CMOS Electrically Erasable PROM

2

FEATURES

- High Speed Performance - 70, 90, 120, 150, 200, 250ns Access Time
- CMOS Technology for Low Power Dissipation
  - 70mA Active
  - 150µA Standby
- Fast Write Cycle Times
  - 64-Byte Page Write Operation
  - Page or Byte Write Cycle - 2ms
  - Average Byte Write Time - 31µs
- High Endurance/Retention
  - 10^4 Erase/Write Cycles
  - >10 Years Data Retention
- JEDEC-Approved
  - Byte Wide Pinout, 28 Pin DIP or 32 Pin Chip Carrier
- Hardware Chip Clear
- Hardware Data Protection
- Software Data Protection
- Write Operation Status
  - RDY/BSY
  - Data Polling
  - Toggle Bit
  - Software Data Protection Status
- Available in Extended Temperature Range:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Military *: -55°C to +125°C

DESCRIPTION

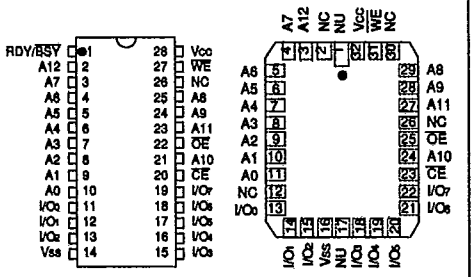
The Microchip Technology Inc. 28C64B is a CMOS 64K bit Electrically Erasable and Programmable Read only Memory. The device is organized as 8K words by 8 bits (8K bytes). An advanced CMOS design and process provides high speed while reducing power requirements. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for wait states.

The 28C64B is accessed like a static RAM for the read or write cycle without the need of external components. During a write operation, the address and 1 to 64 bytes of data are latched internally, freeing the microprocessor address and data bus for other operation. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The completion of a write cycle is detected by either Data polling of output (I/O7) or the Toggle Bit (I/O6).

* See Military Data Sheet DS60037.

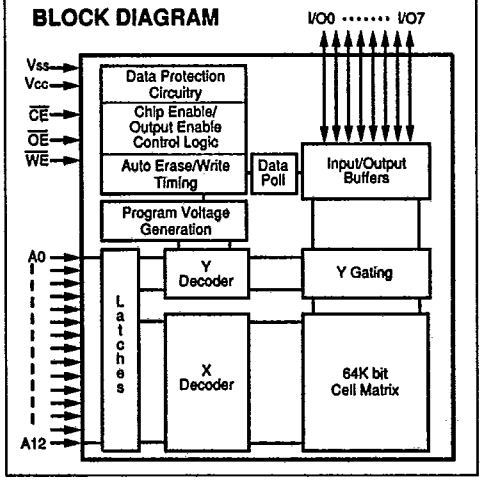
PIN CONFIGURATION

Top View



● Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0-A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0-I/O7	Data Input/Output
Vcc	+5V
Vss	Ground
NC	No Connection: no internal connection
NU	Not used: no external connection is allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc and Input Voltage W.R.T. Vss..... ....-0.6V to 6.25V
All Output Voltage W.R.T. Vss..... ..-0.6V to Vcc +0.6
Voltage of $\overline{OE}$ W.R.T. Vss .....-0.6V to 13.5V
Temperature Under Bias. .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Vcc = +5V ± 10%
TAMB: Commercial: 0°C to +70°C
Industrial: -40°C to +85°C

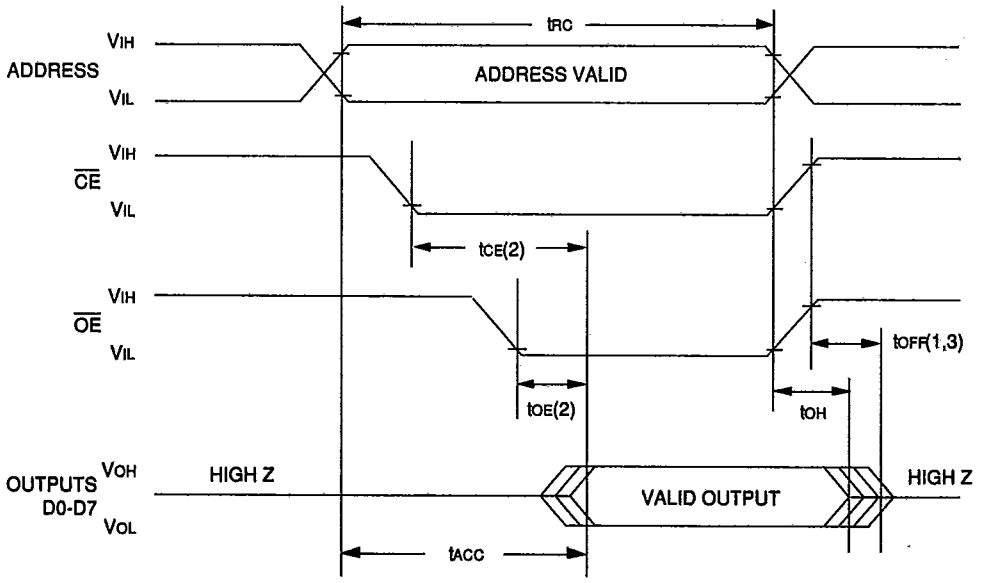
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc +1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = 0V to Vcc +1.0V
Input Capacitance		CI	-	10	pF	VIN = 0V; TAMB = 25°C; f = 1MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4 -	- 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT = 0 to Vcc
Output Capacitance		CO	-	10	pF	VOUT = 0V; TAMB = 25°C; f = 1MHz
Address and Control Capacitance		CIN	-	6	pF	VIN = 0V; TAMB = 25°C; f = 1MHz
Power Supply Current, Active	TTL Input	ICC1	-	70	mA	TAMB = 0°C to 70°C; TAMB = -40°C to 85°C; other conditions: Vcc = 5.5V, max frequency $\overline{OE}$ = $\overline{CE}$ = VIL, IOUT = 0mA, VIL = -0.1V to 0.8V VIH = 2.0V to Vcc
Power Supply Current, Standby	TTL Input CMOS Input	ICC(s)1 ICC(s)3	- -	1 150	mA µA	TAMB = 0°C to 70°C; $\overline{CE}$ = VIH TAMB = -40°C to 85°C; $\overline{CE}$ = VIH all TAMB; $\overline{CE}$ = Vcc ± 0.2V

READ OPERATION
AC Characteristics

Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial: T_{AMB} = 0°C to +70°C
Industrial: T_{AMB} = -40°C to +85°C

Parameter	Symbol	28C64B-70		28C64B-90		28C64B-12		28C64B-15		28C64B-20		28C64B-25		Units	Test
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	70	-	90	-	120	-	150	-	200	-	250	-	ns	
Address to Output Delay	t_{ACC}	-	70	-	90	-	120	-	150	-	200	-	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	-	70	-	90	-	120	-	150	-	200	-	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to O/P Delay	t_{OE}	0	35	0	40	0	50	0	70	0	80	0	100	ns	$\overline{OE}$ = V_{IL}
$\overline{CE}$ or OE to O/P Float	t_{OFF}	0	35	0	40	0	50	0	65	0	70	0	70	ns	
Output Hold From Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0	-	0	-	0	-	0	-	0	-	0	-	ns	

READ WAVEFORM



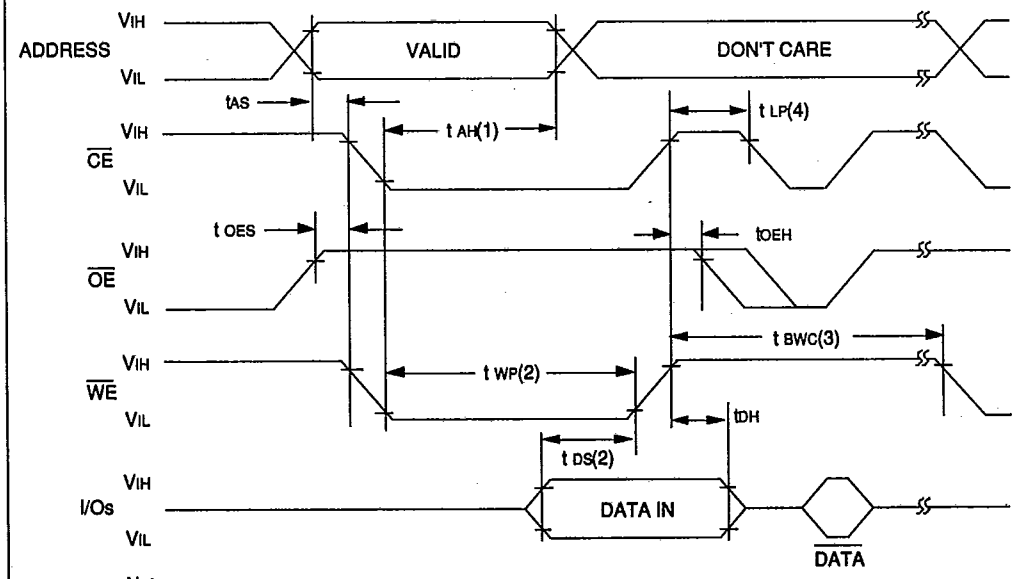
Notes:
(1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
(3) This parameter is sampled and is not 100% tested.

BYTE WRITE AC Characteristics

Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100pF	
Input Rise and Fall Times:	20 nsec	
Ambient Temperature:	Commercial:	T_{AMB} = 0°C to +70°C
	Industrial:	T_{AMB} = -40°C to +85°C

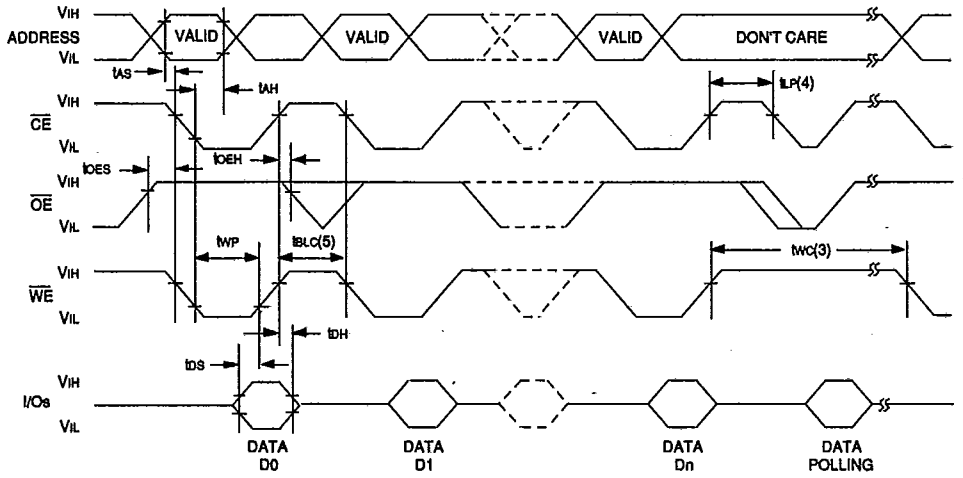
Parameter	Symbol	28C256 - 90/12/15/20/25			Units	Conditions
		Min	Typ	Max		
Write Cycle Time	t_{WC}	-	1	2	ms	-
Byte Write Cycle Time	t_{BWC}	-	1	2	ms	(see Note 3)
Address Set-Up Time	t_{AS}	0	-	-	ns	-
Address Hold Time	t_{AH}	50	-	-	ns	-
$\overline{OE}$ Set-Up Time	t_{OES}	0	-	-	ns	-
$\overline{OE}$ Hold Time	t_{OEH}	0	-	-	ns	-
Data Set-Up Time	t_{DS}	50	-	-	ns	-
Data Hold Time	t_{DH}	0	-	-	ns	-
Write Pulse Width	t_{WP}	100	-	-	ns	-
Byte Load Timer Cycle	t_{BLC}	0.1	-	150	µs	(see Note 5)
Byte Loading Period	t_{LP}	100	-	-	ns	(see Note 4)

BYTE WRITE WAVEFORM



Notes:
(1) t_{AH} is specified from $\overline{CE}$ or $\overline{WE}$ whichever occurs last.
(2) t_{WP} and t_{DS} are specified from $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(3) t_{BWC} and t_{WC} are composed of both the write loading period and the internal programming cycle.
(4) t_{LP} is the minimum time before starting a Read to observe the write operation status bits.
(5) To insure the start of the internal programming cycle t_{BLC} must be extended beyond 100 µs.

PAGE WRITE WAVEFORM



DEVICE OPERATION

The Microchip Technology Inc. 28C64B has five basic modes of operation - read, standby, page or byte write, write inhibit and chip clear - as outlined in the following table.

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	VIL	VIL	VIH	DOUT
Standby	VIH	X(1)	X	High Z
Write (2)				
- Byte/Page	ⓥ	VIH	ⓥ	DIN
Write Inhibit	X	VIL	X	High Z/DOUT
Write Inhibit	VIH	X	X	High Z
Write Inhibit	X	X	VIH	High Z/DOUT
Chip Clear (3)	VIL	VH	ⓥ	High Z

Notes: (1) X = any TTL level
(2) Refer to "Programming Waveforms"
(3) Refer to "Chip Clear Waveforms"
(4) ⓥ = Low going pulse
(5) VH = 12V ± 5%

Read

The read is initiated by presenting a stable address to the memory along with $\overline{WE}$ as high, $\overline{CE}$ as low and $\overline{OE}$ as low. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

Byte Write

The byte write is initiated when $\overline{CE}$ and $\overline{WE}$ are low and $\overline{OE}$ is high. The address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The write data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. The 28C64B performs an auto clear before write. After tLP the write operation status bits are available and the $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ signals may be removed.

Page Write

The page write allows 2 to 64 bytes of data to be written into the 28C64B in one internal programming cycle. Internally, there are 64 byte registers (one page) addressed by A0 through A5. Data is loaded into corresponding registers during the loading period and all data will be written into the specified page of memory at once. Each successive byte load cycles, started by the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, must begin within 150µs from the rising edge of the preceding write control signal ($\overline{WE}$ or $\overline{CE}$). Otherwise, the loading period ends and the internal programming cycle starts. If page address (A6 through A12) does not stay the same through the entire loading period, all data loaded will be written into the page address of the last data written. Only those bytes which have been loaded will be programmed. The unselected bytes in the page will not receive a programming cycle, and thus the endurance of the array is preserved. After tBLP the write operation status bits are available and the $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ signals may be removed.

Write Operation Status Bits

The 28C64 provides the user four write operation status bits. RDY/$\overline{BSY}$ pin is used for write cycle status, I/O7 is used for $\overline{Data}$ Polling. I/O6 is used as a Toggle Bit, and I/O3 is used for software data protect status bit.

$\overline{Data}$ Polling: During the write loading period and the internal programming cycle and attempted read results in the complementary of the last data on I/O7. Once the internal programming cycle is completed, true data is available.

RDY/$\overline{BSY}$: The 28C64B has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C64B is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C64B has completed writing and is ready to accept another cycle.

Toggle Bit: During the write loading and the internal programming cycle I/O6 will toggle on each attempted read. The first read value is "0". The toggle operation will cease after completion of the internal programming cycle.

Page Load Timer (I/O5)

During the write loading period and internal programing cycle, I/O5 will show the page-load timer status on read operation. "O" means it is still in the loading window. "I" tells the user that the loading period has expired and the internal programming cycle has begun.

Software Data Protect Status Bit: During the write loading period and internal programming cycle I/O3 will show either a "1", meaning the chip is software data protected or a "0", meaning the chip is not in the software data protection mode.

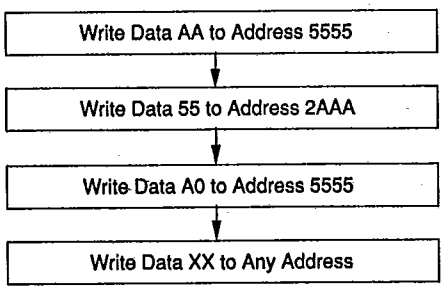
Hardware Data Protection

The 28C64B offers protection against inadvertent write operations by the following hardware features: (1) if VCC is below 3 volts the write operation is inhibited; (2) after VCC is above 3.8 volts, the 28C64B will automatically wait 5ms until a write operation is allowed; (3) a filter circuit on $\overline{WE}$ or $\overline{CE}$ prevents pulses of less than 20ns duration from initiating a write cycle; and (4) holding $\overline{WE}$ or $\overline{CE}$ high, or $\overline{OE}$ low inhibits a write cycle.

Software Data Protection

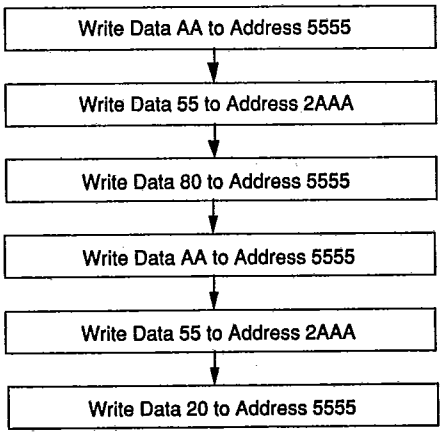
The 28C64B offers a software-controlled data protection feature. Once software data protection is employed, the 28C64B is automatically protected during power-up or power-down without the need for external circuitry. The 28C64B is further protected from inadvertent and accidental writes in the power on state. Setting the software data protection mode requires a series of three bytes of data to be written consecutively into three specific addresses. The write sequence must conform to the page write timing specifications. Figure 1 shows the sequence of setting the software data protect mode. The third byte of the algorithm effectively opens the page write window to enable up to 64 bytes of data to be written. Once the internal programming cycle is complete, the 28C64B will automatically be returned to the software data protection state. Addition writes into a protected device requires the complete software data protection setting sequence to be executed. The soft-

FIGURE 1 SOFTWARE DATA PROTECTION SETTING SEQUENCE



Note: After time twc the 28C64B will automatically enter the soltware data protection state.

FIGURE 2 SOFTWARE DATA PROTECTION RESETTING SEQUENCE



ware data protection circuit can be reset by performing a series of six byte writes as shown in Figure 2. Page writing is allowed immediately after the sixth write of the reset algorithm.

Hardware Chip Clear

he 28C64B array is cleared to all "1"s by raising $\overline{OE}$ to 12V and setting $\overline{CE}$ to VIL and then bringing the $\overline{WE}$ to VIL. See Figure 3.

Software Chip Clear

The 28C64B also provides a software-controlled chip clear feature. The memory can be cleared by issuing a series of six-byte codes to specific addresses. The software chip clear algorithm is shown in Figure 4. The software chip clear functions only when write protection is reset. During the 10ms chip clear cycle, both data polling and toggle bit features can be used to detect the internal programming status.

2

FIGURE 3 HARDWARE CHIP CLEAR

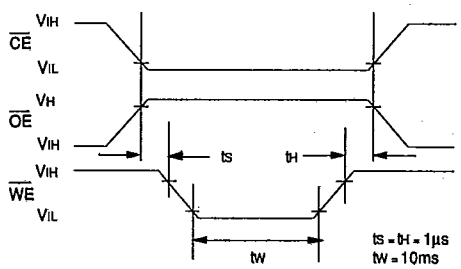
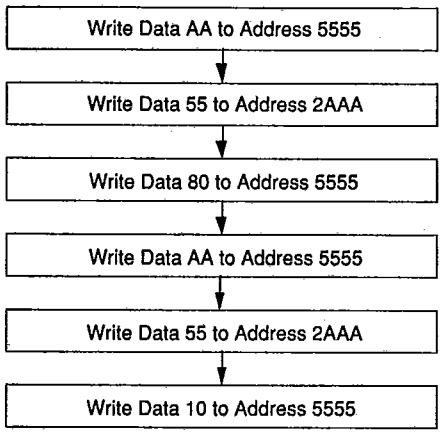


FIGURE 4 SOFTWARE CHIP CLEAR SEQUENCE



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C64B - 15 I/J

Package:	J	Cerdip
	D	Sidebrazed Ceramic Dip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic Dip
Temperature Range:	Blank	0°C to 70°C
	I	-40°C to 85°C
Speed:	90	90ns
	12	120ns
	15	150ns
	20	200ns
	25	250ns
Device:	28C64B	256K (8K x 8) CMOS EEPROM

